Amendments to the Drawings

Figures 1-5 are being amended by adding the label "Prior Art."

Attachment: Replacement Sheet

Annotated Marked-Up Drawings

REMARKS

Claims 1-25 are pending in this Application, of which Claims 1, 7, 12, 14, 18 and 22 are the independent claims. All claims stand rejected.

Claims 1 and 12 are being amended to further clarify the scope of the invention, by replacing the term "plurality of input and output ports" with "plurality of input ports." Support for this amendment is found at least on page 10, lines 10-16 and Fig. 7 of the Specification as originally filed.

Claims 7 and 14 are being amended as indicated in the claim listing above.

Double Patenting

Claims 1-25 have been rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 3, 17, 18, 25 and 31 of U.S. Patent No. 6,590,901. A Terminal Disclaimer is being filed concurrently with this Amendment to disclaim any terminal part of a patent that may issue from the Application that extends beyond the expiration of U.S. Patent No. 6,590,901. Accordingly, the double patenting rejection of Claims 1-25 is believed to be overcome.

Rejection of Claims 12, 13 and 16 under 35 U.S.C. § 112

Claims 12, 13 and 16 have been rejected under 35 U.S.C. § 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter regarded as the invention. Claims 12 and 16 have been amended by correcting the claim terms regarded as lacking antecedent basis. Thus, the § 112 rejection of Claims 12, 13 and 16 is believed to be overcome.

Rejection of Claims 1-25 under 35 U.S.C. 102(b) and 35 U.S.C. 103(a)

Claims 1, 2, 7, 12, 14, 18 and 22 have been rejected under 35 U.S.C. 102(b) as being anticipated by Toda et al. (U.S. Patent No. 5,612,925). Claims 3-6, 8-11, 13, 15-17, 19-21 and 23-25 have been rejected under 35 U.S.C. 103(a) as unpatentable over Toda, alone or in view of Zuravleff et al. (U.S. Patent No. 5,867,735). Applicant respectfully disagrees for the reasons set forth below, and reconsideration is requested.

Claim 1 is directed to a packet buffer random access memory (PBRAM) device. An example PBRAM device is illustrated in Fig. 7 and is not intended to limit the scope of the invention, being defined by the claims. Here, the PBRAM device 62 includes a memory array 74, a plurality of input ports 70 (I/O Port 0 – I/O Port 31), and a plurality of serial registers 72 associated with the input ports 70 (serial register 0 – serial register 31). The serial registers 72 each receive packet data from one of the associated ports 70 and write the packet data to the memory array 74 (see Specification, page 4, lines 3-11). Each of the serial registers 72 is further segmented into a plurality of segments, each segment being associated with corresponding portions of the memory array 74. Such a configuration is illustrated in Fig. 8, where a serial register 72 is divided into segments of 256 bits each. Further, each segment of the serial register 72 may simultaneously transfer data, via a corresponding multiplexor 76, to its corresponding segment of the memory array 74.

Claim 12 is directed to a PBRAM device having a plurality of input ports, further including a plurality of command ports and a memory management unit. As shown in Fig. 7, for example, a plurality of ports 70 are coupled to a memory array 74 by serial registers 72. A plurality of command ports 76 receive commands for operations to be performed in relation to the data conveyed on the input ports (Specification, page 21, lines 2-15). Further, a memory management unit 75 establishes input queue structures within the memory array 74 (page 13, line 23-page 14, line 4).

Toda discloses a memory device for transferring data to and from a memory. As shown in Fig. 16, the memory device 161 includes a memory cell 162, a serial register 167 (the label "164" is a typographical error; see col. 12, lines 25-28), and a data I/O port 164. The serial register 167 has 8 bits. During a typical write operation, data received at the I/O port is transferred serially into the serial register 167. Once an address of the memory cell 162 is selected, the serial register 167 transfers the 8 data bits simultaneously into the memory cell at the selected address (col. 12, lines 17-33).

Toda fails to teach or suggest the claimed invention because Toda relates to providing a memory for a single input/output (I/O) port. Specifically, Toda does not disclose a plurality of input ports. Toda merely discloses a single I/O port 164 that sends and receives data serially. This function is shown at Fig. 17, where signals Dout and Din show data signals into and out of a

single I/O port 164 (col. 12, lines 63-67). Toda also fails to disclose a plurality of serial registers. As shown in Toda, Fig. 16, only a single serial register 167 (erroneously labeled "164") is shown, and no additional serial registers are suggested. It can be seen, then, that Toda discloses a single I/O port 164 that receives data to a single serial register 167, where it is transferred in parallel to a memory 162.

Thus, Toda is comparable to a prior-art dedicated port memory architecture, where each port is associated with a separate, dedicated memory (see Specification at page 2, line 25 – page 3, line 6). In contrast, embodiments of the invention provide for a memory array that is shared by a plurality of input ports. No such embodiment is disclosed or suggested by Toda.

For at least the above reasons, Toda does not disclose the invention as recited in base Claims 1, 7, 12, 14, 18 and 22. Claim 2 depends from base Claim 1 and so inherits the limitations of Claim 1. Accordingly, the § 102 rejection of Claims 1, 2, 7, 12, 14, 18 and 22 is believed to be traversed.

Due to the aforementioned shortcomings of Toda, one skilled in the art would find no suggestion of the invention as recited in dependent claims 6, 11, 13, 17, 21 and 25. Thus, the § 103 rejection of claims 6, 11, 13, 17, 21 and 25 is traversed.

Claims 3-5, 8-10, 15, 16, 19, 20, 23 and 24 depend from one of base Claims 1, 7, 12, 14, 18 and 22, and thus are distinct from Toda for the aforementioned reasons. Zuravleff provides no suggestion of a plurality of input ports for receiving packet data that is stored to a shared memory. Therefore, no combination of Toda and Zuraleff teaches or suggests the present invention, and the § 103 rejection of Claims 3-5, 8-10, 15, 16, 19, 20, 23 and 24 is believed to be overcome; Applicant respectfully requests reconsideration.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By _____

James M. Smith
Registration No. 28,043
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

Concord, MA 01742-9133

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